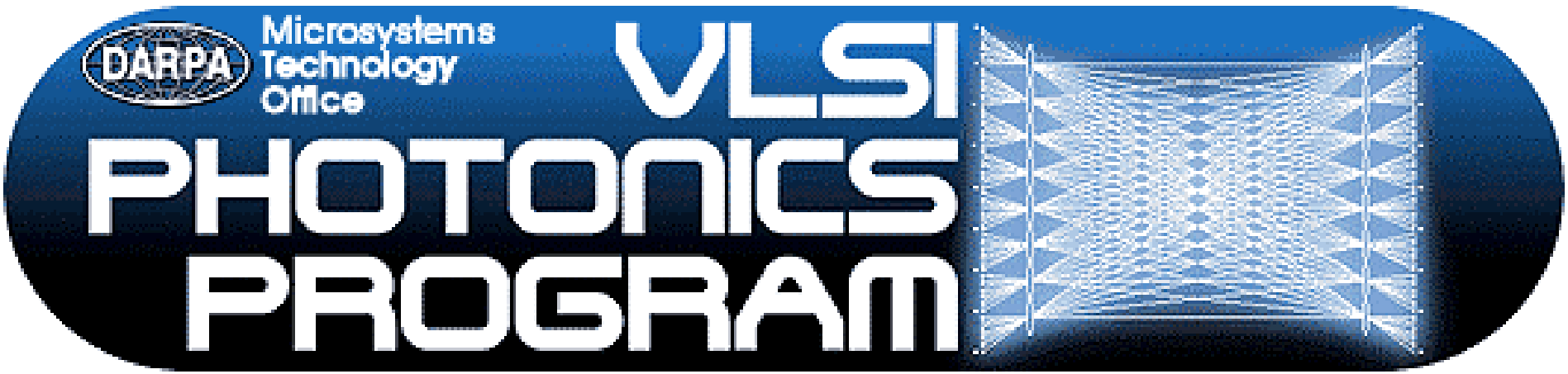
FY01 Review



Dr. Daniel J. Radack

Los Angeles, CA

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Daniel J. Radack, Program Manager

- **Programs:**
  - Advanced Packaging and Interconnects
  - Low Power Electronics
  - High Power Solid State Electronics
  - Advanced Microelectronics (AME)
  - Heterogeneous Integration on Silicon (HGI)
  - Focus Center Research Program (FCRP)
  - VLSI Photonics
  - Heat Removal by Thermo-Integrated Circuits (HERETIC)
  - Technology for Efficient, Agile Mixed Signal Microsystems (TEAM)
- **Background:**
  - 4 years PM in ETO/MTO
  - Semiconductor and integration technologies

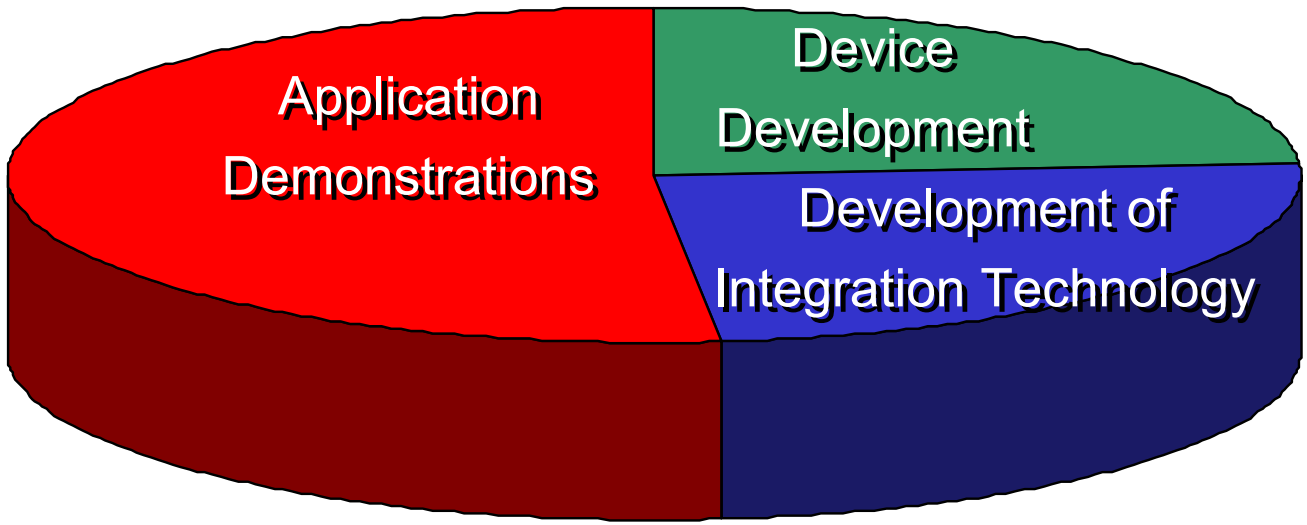
Program Status

- Program Dates: FY98 – FY01
- Most projects in end game.
- Program Status:
  - Transition of core technologies?
  - Where else are VLSI technologies going?

Program Structure

- 16x16 optoelectronic switch at 250 MHz
- shared memory throughput 1 Gbps per link with an aggregate of 32 Gbps
- 20 ms FFT (1024X1024)

- optimize growth of VCSELs for best yield
- integration of VCSELs, detectors and micro-optics



- 2-D array of 16X16 chip
- technologies for scalability to 100x100
- tile 16x16 smart pixel chips to larger size arrays

$56 Million Questions

- What are the military needs for a new integrated photonics/electronics program?
- What are the good technical opportunities that ought to be pursued?

Why Are We Here?

- Review contracted efforts
- Exchange information in community
- Identify breakthroughs
- Discuss future directions

Things To Cover

- What are you trying to do?
- How are you doing it, what is unique/innovative in the approach?
  - Size of VCSEL/detector array
  - Threshold current
  - Throughput/performance
- Where are you?
- Meet with me if you have any open issues or will require any contractual modifications